UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,944,567 B2
APPLICATION NO. : 10/600148
DATED : September 13, 2005
INVENTOR(S) : Raymond J. Beffa

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page:

In ITEM (54) "Title,"	LINE 3,	change "ICS" to --ICs--

In the drawings:

In FIG. 2,		at the reference numeral "**28**" change "IC'S" to --ICs-- at the reference numeral "**34**" change "IC'S" to --ICs--

In the specification:

COLUMN 1,	LINE 3,	change "ICS" to --ICs--

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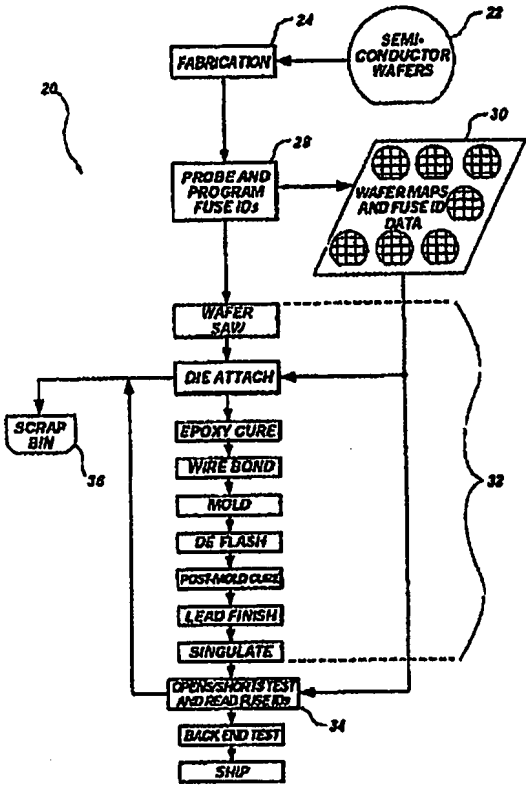
Title page

Replace FIG. 2 with the following Fig. 2



Signed and Sealed this

Sixth Day of November, 2007

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Beffa

(10) **Patent No.: US 6,944,567 B2**
(45) **Date of Patent: *Sep. 13, 2005**

(54) **METHOD IN AN INTEGRATED CIRCUIT (IC) MANUFACTURING PROCESS FOR IDENTIFYING AND REDIRECTING ICS MIS-PROCESSED DURING THEIR MANUFACTURE**

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(73) Assignee: Micron Technology, Inc., Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: 10/600,148

(22) Filed: Jun. 19, 2003

(65) Prior Publication Data

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Related U.S. Application Data

(63) Continuation of application No. 10/067,728, filed on Feb. 4, 2002, now Pat. No. 6,594,611, which is a continuation of application No. 09/793,938, filed on Feb. 27, 2001, now Pat. No. 6,363,329, which is a continuation of application No. 09/537,839, filed on Mar. 29, 2000, now Pat. No. 6,208,947, which is a continuation of application No. 09/302,338, filed on Apr. 29, 1999, now Pat. No. 6,067,507, which is a continuation of application No. 08/806,442, filed on Feb. 26, 1997, now Pat. No. 5,915,231.

(51) Int. Cl.[7] G06F 19/00; G06G 7/6466

(52) U.S. Cl. 702/119; 702/118; 702/82; 700/116; 700/224; 700/226

(58) Field of Search 702/118, 119, 702/117, 81, 82, 87, 84; 700/224, 226, 116, 95, 109, 115, 117; 438/5, 10, 14, 16, 17; 209/573, 571

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(57) **ABSTRACT**

A method of manufacturing IC devices from semiconductor wafers includes providing the wafers and fabricating ICs on the wafers. At probe, a unique fuse ID is stored in each IC, and an electronic wafer map is electronically stored for each wafer indicating the locations of good and bad ICs on the wafer and the fuse IDs of the ICs on the wafer. Each IC is then separated from its wafer to form an IC die, and the IC dice are assembled into IC devices. At the opens/shorts test at the end of assembly, the fuse ID of each IC in each device is automatically retrieved so the wafer map of the IC device may be accessed and evaluated to identify any IC devices containing bad ICs that have accidentally been assembled into IC devices. Any "bad" IC devices are discarded while remaining IC devices continue on to back-end testing.

19 Claims, 2 Drawing Sheets